

BURROUGHS CORPORATION RESEARCH CENTER

TO: *Don R.*

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WORKS

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CONFIDENTIALDate: 4/22/60NORTHVILLE MEMORY DEVICEGeneral Description:

The Northville device is essentially a small memory designed to operate at teletype speeds. The storage capacity of this memory is 2560 bits, organized as 2560-one bit words. The memory operation is a modified coincident-current scheme, the modification being permissible because of the unusual bit length (one bit/word). The device operates in five general modes which are described as follows:

- a) OFF - all power off.
- b) STANDBY - Power on, with various biases applied to prepare the device for proper use.
- c) RECEIVE - to write information into the memory.
- d) IDLE - the device generates idling characters - (one start baud followed by all marks).
- e) TRANSMIT - this position performs two functions
 - 1) It reads the information out of the memory and restores it again,
 - or and 2) It clears the memory.

The device contains seven general circuit functions which are listed and briefly described below.

- a) Power Supply and Switch. The power supply converts either a two high dry cell battery voltage (3v) or a two high NICAD battery voltage (2.5v) into four regulated and two unregulated voltages. The switch selects the various modes of operation supplying bias voltages to pertinent areas to achieve the desired mode.
- b) Keyer. The keyer circuits consist of 12 manual keys, each key generating different information. The keyer is used in the RECEIVE mode for placing information into the memory.

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- c) Logic. The logic circuits are, as the name implies, used to provide the required logical functions for the various modes of operation.
- d) Address. The address circuits are a system of counters used to address the memory proper and install and retrieve memory information in a sequential fashion.
- e) Drivers. The driver circuits generate the currents necessary for switching the ferrite memory cores and, when properly addressed, deliver these currents to the selected memory word.
- f) Memory proper and sense amplifier. The memory proper consisted of 2560 ferrite cores (one core per word) and associated selection diodes. Each core stores one bit of information. The sense amplifier detects the core outputs when the memory is interrogated and amplifies these outputs to a usable level.
- g) Output Buffer and Indicator. The output buffer is also as its name implies, giving a buffer information output to other equipment used with this device. The indicator circuit containing a light bulb performs three functions.
 - 1) It indicates when contact has been made in depressing the keys in the keyer circuit.
 - 2) It gives a rough indication of proper device operation during IDLE, and.
 - 3) It indicates the end of the message during TRANSMIT of information.

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And when writing a ONE, the above equations are applied to negative currents.

When writing a ZERO, no currents are turned on, thereby eliminating the equation to perform this function. From the read equations, using the 1/3 and 2/3 currents as specified in the equations, we have

$$2/3 - 1/3 = 1/3 \text{ (no switching current)}$$

$$2/3 - 1/3 = 1/3 \text{ (no switching current)}$$

$$2/3 + 2/3 - 1/3 = 1 \text{ (switching current)}$$

respectively. This gives the 3 to 1 ratio.

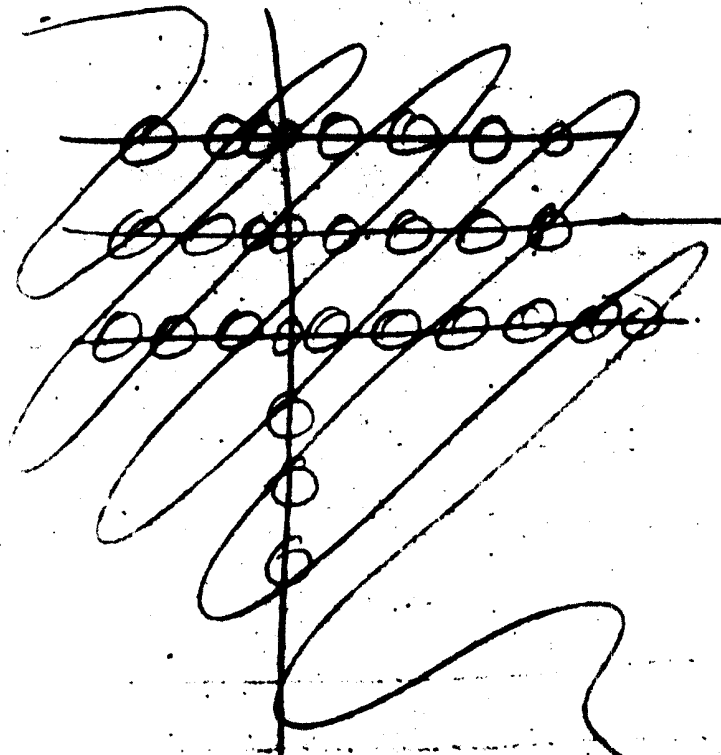
The mechanization of this modified coincident-current scheme is shown in Figure 1. The ferrite cores are arranged in a $64 \times 10 = 2560$ matrix. An 8×8 Driver-Switch combination delivers the X currents and a 4×10 driver-switch combination delivers the Y currents. The bias current is delivered to all cores in the matrix via a single line threading all the cores.

$4 dr + Sw.$

40 lines.

$8 dr + Sw$

lines



$8 dr + Sw$

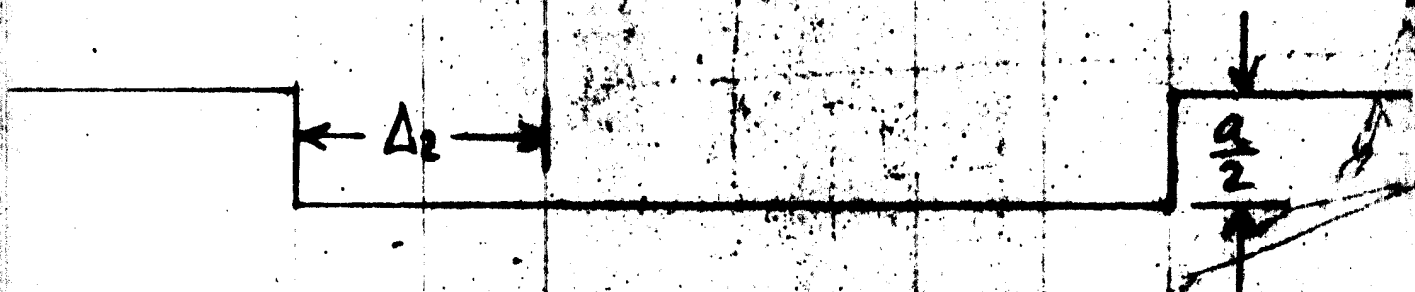
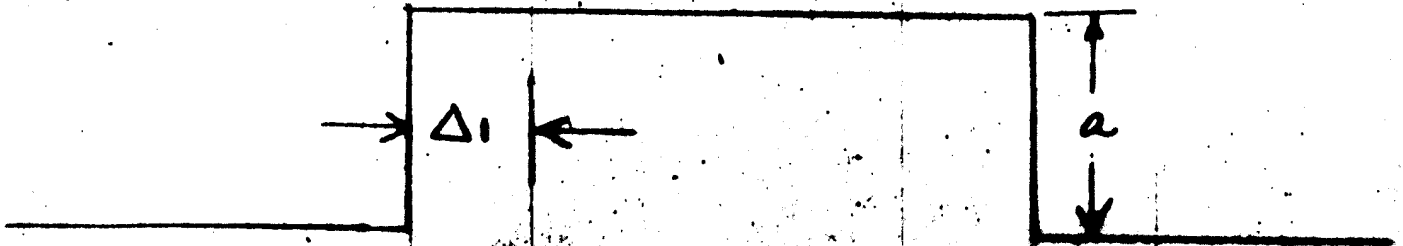
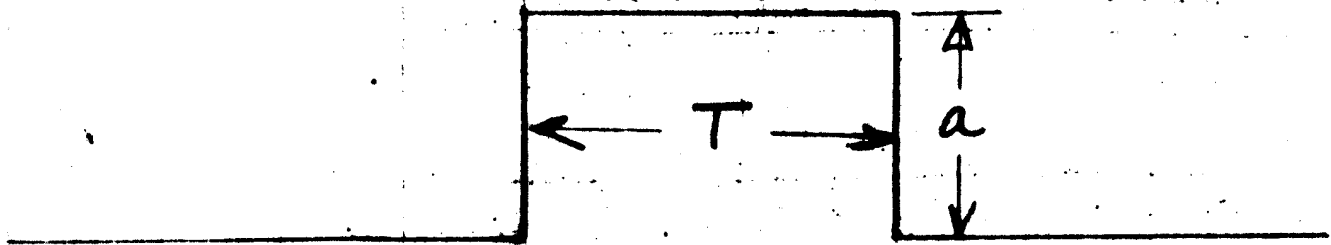
Bias

$10 dr + Sw.$

FIG 1

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